REMARKS

This is in full and timely response to the above-identified Office Action. The above listing of the claims replaces all prior versions, and listings, of claims in the application. Reexamination and reconsideration in light of the proposed amendments and the following remarks are respectfully requested.

Rejections under 35 USC § 103

1) The rejection of claims 1, 3, 4, 8, 9, 11 and 15 under 35 USC § 103(a) as being unpatentable over Souri et al. in view of Millar, Jr., is respectfully traversed.

Inasmuch as the rejection is made under the § 103 statute the disclosure of each reference must be taken as a whole. Souri et al. does not disclose a surge suppression circuit. Instead, it discloses a positive temperature coefficient (PCT) circuit which is designed to respond to temperature and reduce current flow to a reduced level in response to the detection of excess temperature.

Column 1, lines 10 – 23, of Souri et al. discloses:

> PTC_r circuit protection devices are well known. The device is placed in series with a load, and under normal operating conditions, is in **a low temperature, low resistance state**. However, if the current through the PTC_r device increases excessively, and/or the **ambient temperature** around the PTC_r device increases excessively, then the PTC_r device will be "tripped," i.e., converted to a high resistance state such that the current is reduced substantially to a safe level. Generally, the PTC_r device will remain in the tripped state, even if the fault is removed, until **the device has been disconnected from the power source and allowed to cool**. After the current and/or temperature return to their normal levels, the PTC_r device will switch back to the low temperature, low resistance state.

> An example of a PTC_r device is one that contains a PTC_r composition which is composed of a PTC conductive polymer. The **largest steady state current** which will not cause any of the devices in a batch of devices to trip is referred to as the "hold current" (I_{hold}), and the **smallest steady state current** which will cause all of the devices to trip is referred to as the "trip current" (I_{trip}). In general, **the difference between I_{hold} and I_{trip} decreases slowly as the ambient temperature increases**, and the higher the ambient temperature, the lower the hold current and the trip current. (Emphasis added)

As will be appreciated, there is no disclosure of this circuit being responsive to spikes in voltage/current, but rather to the temperatures which result from either excessively high currents and/or ambient temperatures. The response characteristics of the disclosed circuits are shown in terms of current and voltage. Time is not a factor that is considered. It is therefore submitted that one or more spikes in voltage/current could possibly occur before the temperature would rise to a level where the circuit would trip. This tendency would possibly be enhanced by a low ambient temperature.

It is therefore submitted that the rejection relies on a primary reference which fails to disclose one of the basic elements that is claimed – that is to say, a surge suppressing circuit. Accordingly, it cannot be relied upon to suggest a surge suppressing circuit which uses a complementary Darlington pair as per the claimed requirements.

It is again stressed that this rejection is not made under § 102 wherein the claims can be read on disclosed circuits with all but total disregard for their function/intention, but is made under § 103 wherein the consideration of the hypothetical person of ordinary skill and the whole disclosure of each reference must be taken into account. Souri et al. reference discloses a number of circuits. Only the circuit shown in Fig. 3B includes a complementary Darlington pair, and this pair is used with a positive temperature coefficient element (PTC) Rp3. This combination of elements cannot be

ignored by the hypothetical person of ordinary skill in that the use of Rp3 element is fundamental to the PTC control which is the basis of the Souri et al. circuits.

In other words, the PTC element cannot be ignored/discarded from the circuit for the sake of rejection. Further, it cannot be assumed for the sake of rejection that the circuits that are shown in Souri et al. are surge suppressing circuits. Moreover, there are no teachings which would suggest that the complementary Darlington pair has any particular merit and thus draw the attention of the hypothetical person of ordinary skill to this particular transistor amplifier configuration.

Miller, Jr. is cited to show a diode. Miller, Jr. does not disclose a complementary Darlington pair. It is advanced for the sake of rejection, that the hypothetical person of ordinary skill would be motivated to introduce a diode such as diode 42 of Miller, Jr., into the circuit arrangement disclosed in Fig. 3B of Souri et al., in order to protect against the transfer of energy due to an inadvertent application of a reverse or wrong polarity on the input, and thus increase the overall protection of the load. However, the circuit which is being cited for the sake of rejection is arranged such that one terminal (T2) is connected to ground. In other words, the circuit of Souri et al. which is being relied upon, is disposed between the load and ground. This is a different situation than that shown in Figs. 1 and 2 of Miller, Jr.

Indeed, Miller, Jr. discloses at column 2, line 63 – column 3, line 8, that diode 42 is disposed in series with the current limiter 44. However, rather than the diode, it is indicated that it is the current limiter 44 which is arranged to prevent currents above a predetermined value from flowing between terminal 20 and 24, regardless of the applied voltage values or loading values, thus also limiting the current which can flow into terminal 24 and the field equipment 14. The current limit value is chosen to be below the critical value which could cause an accident such as an explosion in the hazard area. This section of Miller, Jr. goes on to disclose that terminal 26 is connected to terminal 22 through a circuit 46 that includes a diode 48 and a current limiter 50 which limits the current between terminals 22 and 26 to a predetermined value.

Further, and more importantly, column 1, lines 47 – 63 discloses that a current limiting function is given to the transistor device (e.g. the Darlington pair) by means of a network including a diode circuit connected from the base to the distal end of the emitter

resistor and which diode circuit is characterized by a total number of series diode voltage drops (or the equivalent) equal to the number of diode voltage drops in the base-emitter path plus one, whereby the maximum value of the current which can flow in the main load current path, will be limited to that value which causes the sum of the voltages across the emitter resistor and the emitter-base junction to equal the voltage drop across the diode circuit. The status of the base voltage on the transistors or one of the current limiters is change to a turn-OFF condition in response to the loss of the ground connection.

This renders it clear that if the use of diode 42 of Miller, Jr. were to be contemplated, so would many of the other diodes which are disclosed in connection with the circuit shown in Figs. 1 and 2. Further, in that the circuit of Souri et al. shown in Fig. 3B is not circuited between a "hazardous area" and a "supply source" in the manner that the current limiter circuits of Miller, Jr. are, it is not seen that the teachings which stem from Miller, Jr. would be considered for use in connection with the circuit arrangements disclosed in Souri et al.

In re Keller (642 F.2d 413, 208 USPQ 871 (CCPA 1981)) can be relied upon to teach that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references, taken as a whole, would have suggested to those of ordinary skill in the art.

The citation of Miller, Jr. actually reduces the tenability of the rejection. Miller, Jr. discloses a Darlington pair, not a complementary Darlington pair, and discloses it in the context of current limiting circuits 44 and 60'. This detracts from any merit that may be derived from the fact that one of the plurality of circuits shown in Souri et al. discloses a complementary pair in Fig. 3B. Indeed, of the four circuits which are shown as using Darlington pairs in Souri et al., only one of the four uses a complementary pair. Thus, the combination of Souri et al. and Miller, Jr. is such that there is an clear tendency to use of Darlington pairs as different from the claimed complementary pair.

In this instance, it is neither seen that a *prima facie* case has been established which would properly permit diode 42 of Miller, Jr. to be introduced into the circuit shown

in Fig. 3B of Souri et al., nor has it been established that the PTC circuits of Souri et al. would be considered as suggesting surge suppressing circuits of the nature claimed.

2) The rejection of claims 2,5-7, 10 and 12-14 under 35 USC § 103(a) as being unpatentable over Souri et al. over Miller, Jr. in view of Johnson, is respectfully traversed.

Firstly, this rejection suffers from all of the shortcomings outlined above. Secondly, while there is a Darlington pair arranged with a Zener diode, disclosed in Johnson, note must be had to the fact that this reference further compounds the tendency in the art which has been applied against the claims to use Darlington pairs as different from complementary Darlington pairs. A further problem which is introduced by the citation of Johnson is that it discloses the use of a Zener diode voltage regulator 62 which would appear to the surge suppressing arrangement which is disclosed. More specifically, column 4, lines 9 - 35 discloses:

> The second circuit 56 of the power supply 50 generates a regulated DC signal for powering the control electronics by bootstrapping the normal battery voltage with a signal derived from the 60 volt DC output of the first circuit 54. As shown in FIG. 2, the nominal 12 volt DC signal provided by the battery is applied to the V_{REG} line through a **conventional zener diode voltage regulator 62 and a diode 64.** The 60 volt DC signal provided by the electric power converter 54, on the other hand, is applied to the V_{REG} line through a series-pass voltage regulator 66, and a diode 68. A power supply filter capacitor 70 is connected between the V_{REG} line and ground to filter the power signal.
>
> The **zener diode regulator 62 is included principally to protect the electronic circuitry from excessively high battery voltages**. Regulator 62 includes a series resistor 72 and a shunt zener diode 74. Since the zener voltage of diode 74 is relatively high (e.g., 18 volts), the battery

> voltage will normally be less than the zener voltage and the zener will therefore be nonconductive. The voltage at the output of the regulator 62 will thus normally be approximately equal to the battery voltage. If the battery voltage rises above the zener voltage of the zener diode 74, however, zener diode 74 will become conductive, preventing V_{REG} from exceeding the zener voltage.
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> The **series-pass regulator 66** connected to the 60 volt DC line also includes a zener diode regulator, in this case including a series resistor 76 and a zener diode 78. The series-pass regulator also, however, includes a **Darlington-pair transistor amplifier 80**. The transistor amplifier 80 buffers the voltage appearing across the zener diode 78, enabling the regulator to operate without needless dissipation of excess power. The zener diode 78 used in the series-pass regulator 66 has a zener voltage of approximately 10 volts. The voltage at the output of the second regulator 66 will only be about 8.5 to 9.0 volts, however, due to the voltage drop of between 1.0 and 1.5 volts added by the base-emitter junctions of the two transistors of the Darlington-pair transistor amplifier 80. (Emphasis added)

As will be appreciated, this reference apart from teaching the use of a Darlington pair as different from the claimed complementary pair, also discloses the use of a surge suppressing circuit which is comprised of a resistor 72 and a zener diode, and which is devoid of a transistor amplifier. The combination of Souri et al. Miller, Jr. and Johnson, therefore cannot establish a *prima facie* case of obviousness and thus cannot be relied upon to render the claimed subject matter unpatentable.

Conclusion

It is respectfully submitted that the claims as they stand before the PTO are allowable for at least the reasons advanced above. Favorable reconsideration and allowance of this application are courteously solicited.

Respectfully submitted,

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